CLAIMS:

1. A method of fabricating a complementary metal oxide semiconductor (CMOS) field effect transistor, comprising the steps of:

(a) providing a substrate;

(b) providing on said substrate a polysilicon layer formed upon a gate dielectric layer of a gate structure of the transistor;

(c) doping the polysilicon layer using at least one dopant;

(d) forming a polysilicon gate electrode of the gate structure;

(e) depositing on the polysilicon gate electrode at least one of a metal and an alloy; and

(f) siliciding the polysilicon gate electrode to form a silicide adjacent to said gate dielectric layer.

2. The method of claim 1, wherein the doping step (c) is performed after the forming step (d).

3. The method of claim 1, wherein the at least one dopant comprises at least one of As, P, B, Sb, Bi, In, Tl, Al, Ga, Ge, Sn and N_2.

4. The method of claim 1, wherein the doping step (c) dopes the polysilicon layer using Sb as said at least one dopant.

5. The method of claim 1, wherein the doping step (c) dopes the polysilicon layer using an ion implantation process.

6. The method of claim 5, wherein the doping step (c) dopes the polysilicon layer using a pre-determined dose in a range from about $1x10^{14}$ to $4x10^{15}$ ions/cm^2.

7. The method of claim 1, wherein the forming step (d) further comprises the step of:

amorphizing the polysilicon gate electrode.

8. The method of claim 7, wherein said amorphizing step comprises the step of:

performing an ion implantation process using at least one of Si and Ge.

9. The method of claim 1, wherein said at least one of the metal comprises at least one of Ni, Co, Pt, Ti, Pd, W, Mo, and Ta.

10. The method of claim 1, wherein said at least one of the metal comprises Ni.

11. The method of claim 1, wherein said at least one of the metal comprises Co.

12. The method of claim 1, wherein said at least one of the alloy comprises at least one of C, Al, Ti, V, Cr, Mn, Fe, Co, Ni, Cu, Ge, Zr, Nb, Mo, Ru, Rh, Pd, Ag, In, Sn, Hf, Ta, W, Re, Ir, and Pt.

13. The method of claim 1, wherein said siliciding step employs an annealing process.

14. The method of claim 13, wherein the annealing process is performed at a substrate temperature of about 350 to 750 degrees Celsius for a duration of about 0.3 to 30 min.

15. The method of claim 13, wherein the annealing process forms at least one monolayer of the at least one dopant at an interface between the gate dielectric layer and the silicide to control work function and electron mobility in the silicide.

16. A complementary metal oxide semiconductor (CMOS) field effect transistor formed on a substrate using a method, comprising:

(a) providing a substrate;

(b) providing on said substrate a polysilicon layer formed upon a gate dielectric layer of a gate structure of the transistor;

(c) doping the polysilicon layer using at least one dopant;

(d) forming a polysilicon gate electrode of the gate structure;

(e) depositing on the polysilicon gate electrode at least one of a metal and an alloy; and

(d) siliciding the polysilicon gate electrode to form a silicide adjacent to said gate dielectric layer.

17. The transistor of claim 16, wherein the doping step (c) is performed after the forming step (d).

18. The transistor of claim 16, wherein the at least one dopant comprises at least one of As, P, B, Sb, Bi, In, Tl, Al, Ga, Ge, Sn and N_2.

19. The transistor of claim 16, wherein the doping step (c) dopes the polysilicon layer using only Sb.

20. The transistor of claim 16, wherein the doping step (c) dopes the polysilicon layer using an ion implantation process.

21. The transistor of claim 20, wherein the doping step (c) dopes the polysilicon layer using a pre-determined dose in a range from about $1x10^{14}$ to $4x10^{15}$ ions/cm^2.

22. The transistor of claim 16, wherein the forming step (d) further comprises the step of:

amorphizing the polysilicon gate electrode.

23. The transistor of claim 22, wherein said amorphizing step comprises the step of: performing an ion implantation process using at least one of Si and Ge.

24. The transistor of claim 16, wherein said at least one of the metal comprises at least one of Ni, Co, Pt, Ti, Pd, W, Mo, and Ta.

25. The transistor of claim 16, wherein said at least one of the metal comprises Ni.

26. The transistor of claim 16, wherein said at least one of the metal comprises Co.

27. The transistor of claim 16, wherein said at least one of the alloy comprises at least one of C, Al, Ti, V, Cr, Mn, Fe, Co, Ni, Cu, Ge, Zr, Nb, Mo, Ru, Rh, Pd, Ag, In, Sn, Hf, Ta, W, Re, Ir, and Pt.

28. The transistor of claim 16, wherein said siliciding step employs an annealing process.

29. The transistor of claim 28, wherein the annealing process is performed at a substrate temperature of about 350 to 750 degrees Celsius for a duration of about 0.3 to 30 min.

30. The transistor of claim 28, wherein the annealing process forms at least one monolayer of the at least one dopant at an interface between the gate dielectric layer and the silicide to control work function and electron mobility in the silicide.